An Accurate Approach of Nonlinearity Compensation for VSI Inverter Output Voltage

Hengbing Zhao, Q. M. Jonathan Wu, *Member, IEEE*, and Atsuo Kawamura, *Fellow, IEEE*

***Abstract*—An accurate nonlinearity compensation technique for voltage source inverter (VSI) inverters is presented in this paper. Because of the nonlinearity introduced by the dead time, turn-on/off delay, snubber circuit and voltage drop across power devices, the output voltage of VSI inverters is distorted seriously in the low output voltage region. This distortion influences the output torque of IM motors for constant V/f drives. The nonlinearity of the inverter also causes 5th and 7th harmonic distortion in the line current when the distributed energy system operates in the grid-connected mode, i.e., when the distributed energy system is parallel to a large power system through the VSI inverter. Therefore, the exact compensation of this nonlinearity in the VSI inverter over the entire range of output voltage is desirable. In this paper, the nonlinearity of VSI inverter output voltage and the harmonic distortion in the line current are analyzed based on an open-loop system and a L–R load. By minimizing the harmonic component of the current in a d-axis and q-axis synchronous rotating reference frame, the exact compensation factor was obtained. Simulations and experimental results in the low frequency and low output voltage region are presented.**

***Index Terms*—Compensation factor identification, dead time, nonlinearity compensation.**

I. Introduction

THE OUTPUT voltage error of voltage source inverter (VSI) inverters and its influence on the torque output of IM motors in the low output voltage region is well known. When the rotor speed is near zero, the frequency and voltage of the stator are very low. As a result, the nonlinearity of VSI inverter output voltage cannot be ignored and should be compensated exactly. There are several factors that distort the output voltage, such as the dead time, turn-on/off delay, voltage drop across the switches, charging, and discharging parasitic capacitance and snubber circuits of power switches. A number of these factors have been analyzed and clarified in detail in literature [1]–[3]. The main nonlinearity of VSI inverters is attributed to the necessary dead time inserted in every pulse-width modulated (PWM) cycle to avoid the short-through of the dc power supply. During this dead time, the output voltage is determined according to the direction of the load current. The turn-on/off delay times for insulated gate bipolar transistor (IGBT) based inverters cannot be neglected and contributes to the nonlinearity in similar fashion, and can be treated as part of the dead time [1], [2]. Another important factor is the voltage drop across the power switches. This voltage drop can be divided into two parts, one part is constant, which is referred to the threshold value; the other is the resistance voltage drop, varying according to the load current, which is caused by the conduct resistance [1]. The conduct resistance, in turn, varies due to temperature changes. For motor control, this conduct resistance can be treated as part of the stator resistance [1], [2]. In this paper, only the voltage errors introduced by the dead time, turn-on/off delay and the voltage drop on the so-called threshold value are considered and compensated.

Various compensation methods have been proposed to improve the output waveforms over the past decade [1]–[13]. One such method is the pulse-based compensation method, in which the error is detected and compensated in the next PWM period [3], [5], [6]. Another method is based on the average-value theory, in which the lost volt–seconds are averaged over an entire PWM cycle and added to the reference voltage according to the direction of the load current [1], [2], [6], [7]. The key challenges of these methods are the correct calculation of the compensation voltage and the accurate detection of the zero current crossing. The compensation voltage can be obtained experimentally via a using startup measurement [1] or calculated according to the dead time and other parameters of the power switches. Considering that the voltage drop across the switches changes with the load current and frequency, an online compensation method was proposed by using a lookup table of experimental data [2].

In this paper, an accurate compensation method is proposed based on the average-value theory. The initial compensation voltage can be evaluated from simple calculation according to the dead time and the PWM period. Introducing a proportional factor into the compensation voltage. This factor is adjusted according to the current harmonics introduced by nonlinearity of VSI inverters, the exact compensation can be obtained by minimizing the effects of the current harmonic components through simple experiment. The zero current crossing is determined simply by using reconstructed current according to the filtered d and q components of the load current in the synchronous rotating reference frame. Using the above method, accurate voltage compensation is possible. The results of simulations and experiments in the low output frequency and low output voltage region are presented to verify the proposed method.

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H. Zhao and Q. M. J. Wu are with the National Research Council, Institute for Fuel Cell Innovation, Vancouver, BC V6T 1W5, Canada (e-mail: hengbing.zhao@nrc.ca).

A. Kawamura is with Yokohama National University, Kanagawa 240-8501, Japan.

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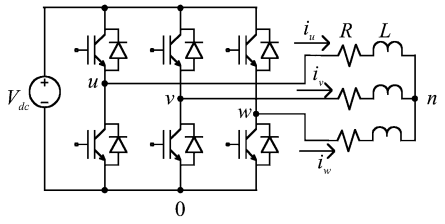

Fig. 1. Three-phase PWM inverters with a R–L load.

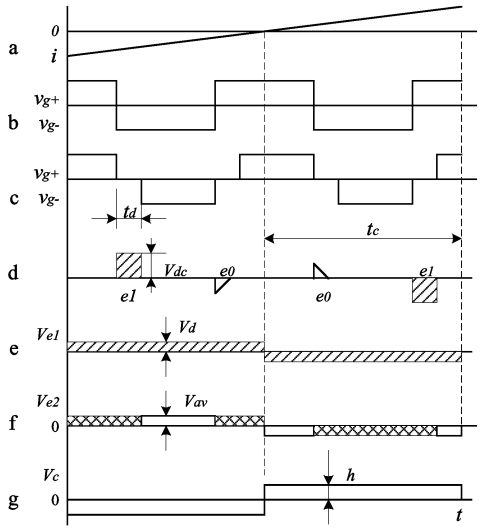

Fig. 2. Analysis of nonlinearity of VSI inverters: (a) phase current, (b) ideal gating pulses of the upper and lower switches of one leg, (c) actual gating pulse with the dead time t_d, (d) volt–second error during the dead time (e_1: caused by the switch, e_0: caused by the antiparallel diode), (e) average voltage error within one PWM period t_c, (f) constant voltage drop across the switch (blank area) and the diode (shaded area), and (g) compensation voltage.

II. Analysis of Non-Linearity of VSI Inverter

Fig. 1 shows the topology of typical three-phase PWM inverters with a R–L load. By comparing the reference voltage with a triangular carrier wave, ideal PWM gating pulses can be obtained, as shown in Fig. 2(b) (for one leg). v_{g+} and v_{g-} denote the gating pulses of the upper and lower switches of one leg. A small time delay, t_d, the so-called dead time, is inserted at the rising edge of the gating pulse and is used to guarantee that both switches in one leg of the inverters never conduct simultaneously [shown in Fig. 2(c)]. Turn-on/off delay of the power switch will also introduce voltage error, which works the same as the dead time. This introduces a load current dependent voltage error e_1 into the ideal output voltage V_{u0} at every PWM period t_c. The parasitic capacitance of the power switches are charged and discharged through the load current, introducing a voltage error e_0 during the dead time when the load current is near zero. e_0 and e_1 are located at the different edge of the PWM pulses [Fig. 2(d)]. Averaging e_1 in the PWM period, average error V_d can be obtained. Output voltage of the inverter can also be distorted by the voltage drop across power switches, which exists during the entire PWM cycle. Here, the voltage drop across the power switches is divided into two parts: a constant part and a variable portion. The constant part is different for every power switch and antiparallel diode, and is represented by the averaging value V_{av}. The error V_{av} is shown in Fig. 2(f),

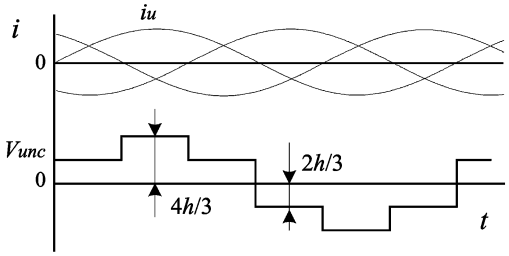

Fig. 3. Compensation voltage for one phase.

where the hatched area denotes the constant voltage drop across the diode. The variable part, which varies according to the load current, is treated as part of the load resistance and will not be considered here. By averaging e_1 in the PWM period, the error introduced to V_{u0} by V_d and V_{av} can be compensated by

$$\begin{aligned} V_{u0c} &= (V_d + V_{av}) \cdot \mathrm{sign}(i_u) \\ &= (V_{dc} \cdot t_d/t_c + V_{av}) \cdot \mathrm{sign}(i_u) \\ &= h \cdot \mathrm{sign}(i_u) \end{aligned} \tag{1}$$

where h is the magnitude of the compensation voltage. Similarly

$$\begin{aligned} V_{v0c} &= h \cdot \mathrm{sign}(i_v) \\ V_{w0c} &= h \cdot \mathrm{sign}(i_w). \end{aligned} \tag{2}$$

The magnitude of the compensation voltage is constant and the sign of the compensation voltage is related to the direction of the phase current, as shown in Fig. 2(g). The phase voltage can be expressed as

$$\begin{aligned} V_{un} &= V_{u0} - V_{n0} \\ &= (2 \cdot V_{u0} - V_{v0} - V_{w0})/3. \end{aligned} \tag{3}$$

Therefore, compensation voltage V_{unc} for phase voltage V_{un} can be expressed by

$$V_{unc} = h \cdot [2 \cdot \mathrm{sign}(i_u) - \mathrm{sign}(i_v) - \mathrm{sign}(i_w)]/3. \tag{4}$$

It follows that the compensation voltage for the u phase output voltage is a six-step wave, as shown in Fig. 3, can be expanded as

$$V_{unc} = \frac{4h}{\pi} \sum_n \frac{1}{n} \sin(nx) \quad (n = 1, 3, 5 \ldots) \tag{5}$$

where x is the phase angle.

Similarly

$$V_{vnc} = \frac{4h}{\pi} \sum_n \frac{1}{n} \sin\left[n\left(x - \frac{2\pi}{3}\right)\right] \tag{6}$$

$$V_{wnc} = \frac{4h}{\pi} \sum_n \frac{1}{n} \sin\left[n\left(x - \frac{4\pi}{3}\right)\right]. \tag{7}$$

If the compensation is exactly correct, there would be no high-order harmonics introduced into the load current. Typically, however, the parameters of the power switches cannot be accurately identified and vary due to the load current. Overcompensation and undercompensation often occur, and both of which generate a six-step voltage error and distort the output voltage and current. Undercompensation, in particular,

also leads to significant current clamping, as discussed in the following section.

Considering a three-phase symmetric inductive load, the relative currents can be expressed as

$$i_u = I(h)\sum_n \frac{1}{n}\sin[n(x-\theta)] \tag{8}$$

$$i_v = I(h)\sum_n \frac{1}{n}\sin\left[n\left(x-\frac{2\pi}{3}-\theta\right)\right] \tag{9}$$

$$i_w = I(h)\sum_n \frac{1}{n}\sin\left[n\left(x-\frac{4\pi}{3}-\theta\right)\right] \qquad n=1,5,7,11,13,17\ldots \tag{10}$$

where $I(h)=(4h/\pi\cdot z(x)), z(x)$ is the load resistance and θ is related to the power factor.

Using frame transformation, the d and q components of the load current introduced by the voltage error in the synchronous rotating reference frame can be expressed as

$$i_d = \sqrt{\frac{3}{2}}I(h)\sum_n \frac{1}{n}\sin[(n\pm 1)x - n\theta] \tag{11}$$

$$i_q = \sqrt{\frac{3}{2}}I(h)\sum_n \left\{\pm\frac{1}{n}\cos[(n\pm 1)x-n\theta]\right\}. \tag{12}$$

$+: n=5,11,17\ldots$

$-: n=1,7,13,19\ldots$

Equations (11) and (12) can be expanded and rewritten as

$$i_d = \sqrt{\frac{3}{2}}I(h)\left[-\sin\theta+\frac{1}{5}\sin(6x-5\theta)+\frac{1}{7}\sin(6x-7\theta) + \frac{1}{11}\sin(12x-11\theta)+\frac{1}{13}\sin(12x-13\theta)+\cdots\right] \tag{13}$$

$$i_q = \sqrt{\frac{3}{2}}I(h)\left[-\cos\theta+\frac{1}{5}\cos(6x-5\theta)-\frac{1}{7}\cos(6x-7\theta) + \frac{1}{11}\cos(12x-11\theta)-\frac{1}{13}\cos(12x-13\theta)+\cdots\right]. \tag{14}$$

From the above analysis, it is obvious that the nonlinearity introduced by the dead time, turn-on/off delay and the constant voltage drop across the power switches will introduce a 6n-th harmonics (n $= 1,2,\ldots$) into the d and q components of the load current, where the magnitude of the harmonics is dependant on the load power factor.

III. Accurate Identification of Compensation Voltage

As mentioned previously, it's generally difficult to calculate or measure the compensation voltage exactly. Assuming h_0 is ideal magnitude of the compensation voltage, overcompensation and undercompensation will introduce 6n-th harmonics into the d and q components of the load current in the synchronous rotating reference frame. The magnitude of the harmonics is proportional to the difference between h and h_0, and is related to the power factor θ. By minimizing the 6n-th harmonics in the synchronous rotating reference frame, exact compensation voltage can be obtained. Fig. 4 illustrates an identification strategy for the compensation voltage. Here,

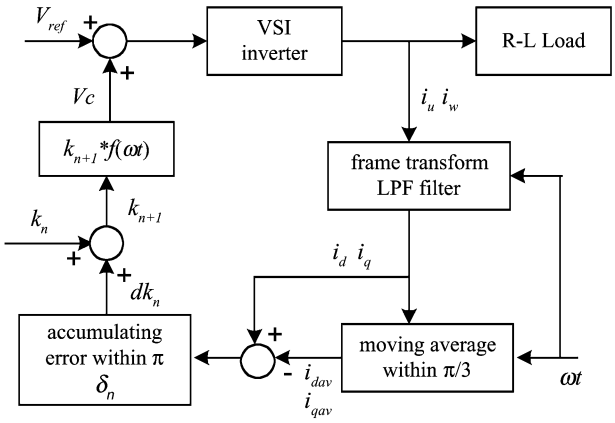

Fig. 4. Identification of compensation factor k.

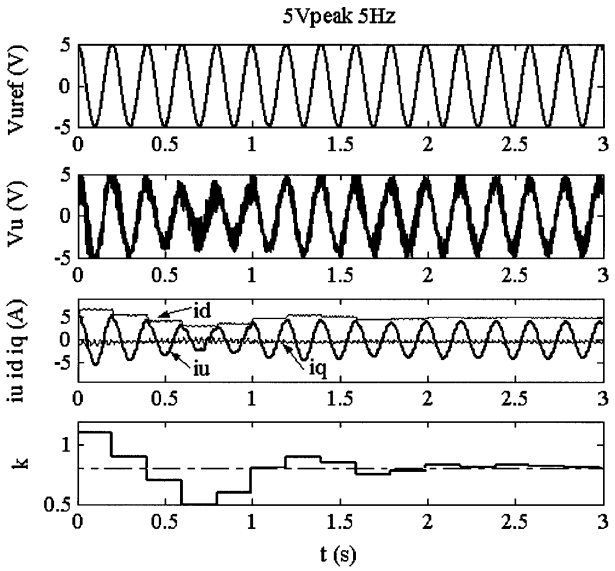

Fig. 5. Identifying compensation factor k by simulation.

a factor k is introduced into the compensation voltage. The moving average method within the region of $\pi/3$ is used to remove the 6n-th harmonics from i_d and i_q components. An average $i_{d\mathrm{av}}$ and $i_{q\mathrm{av}}$ can thus be obtained as the reference value. By integrating the difference between i_d and $i_{d\mathrm{av}}$ or i_q and $i_{q\mathrm{av}}$, the compensation factor k is adjusted until the harmonics satisfies the demand and the factor k stays constant.

In Fig. 4, $f(\omega t)$ is the voltage compensation function (5)–(7), which can be obtained from the direction of the load current and the dead time. The waveform of the compensation voltage is certain, leaving only the magnitude as the unknown. By accumulating the absolute error $|i_q - i_{q\mathrm{av}}|$ or $|i_d - i_{d\mathrm{av}}|$ and comparing with the former value δ_{n-1}, the adjustment direction and size of factor k is modified according to (15)–(16) within every period of reference voltage V_{ref}. To avoid the effect of the change of factor k on the error accumulation, k is adjusted at instant of $\omega t = 0$ according to the accumulating error δ within the region $[\pi, 2\pi]$ of the former period.

$$k_{n+1} = k_n + dk_n \tag{15}$$

$$dk_n = -k'|dk_{n-1}|\cdot \mathrm{sign}(k_n - k_{n-1})\mathrm{sign}(\delta_n - \delta_{n-1}). \tag{16}$$

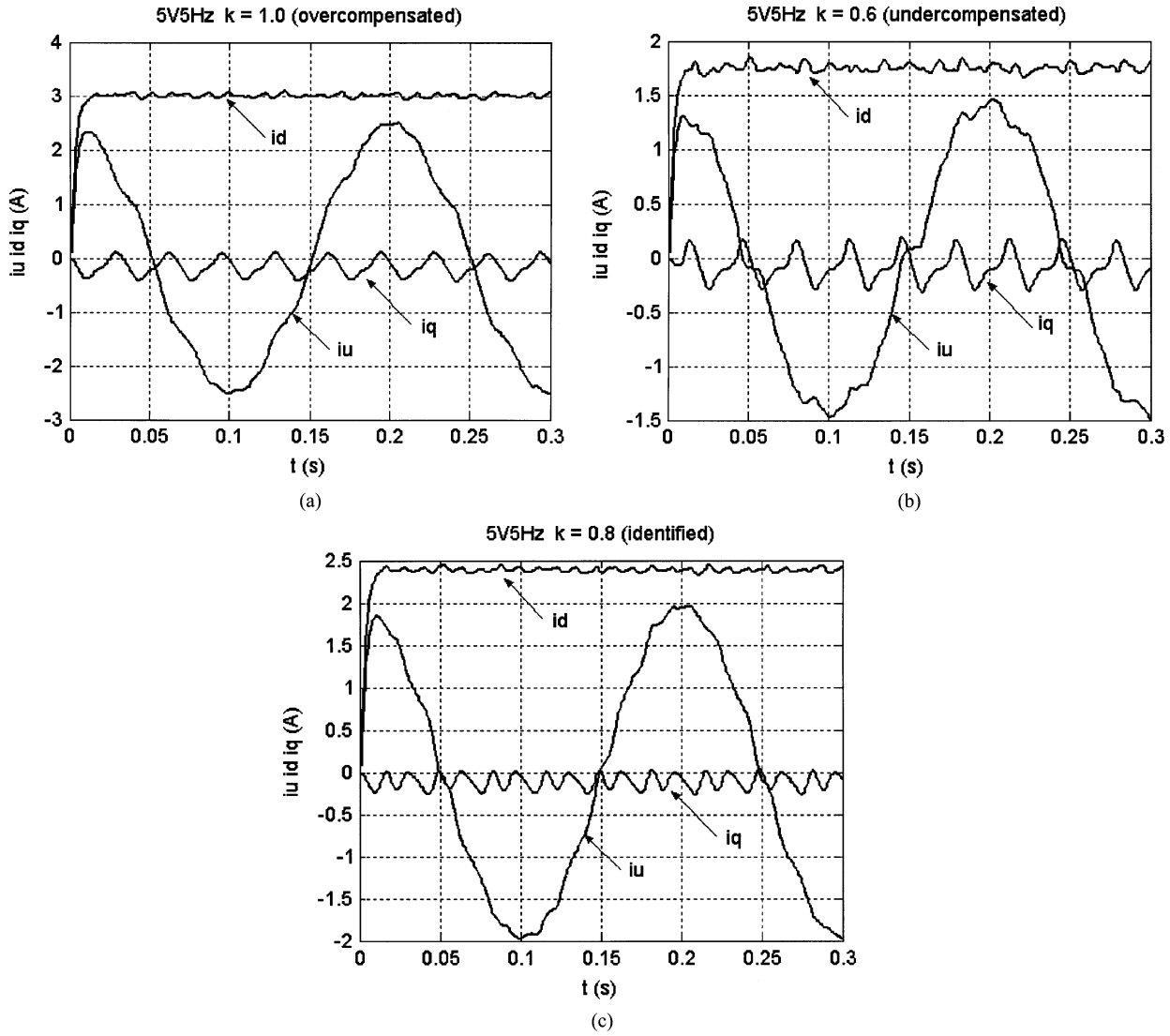

Fig. 6. Simulation results of compensation with $k = 1.0$, 0.6, and 0.8: (a) overcompensation $k = 1.0$, (b) undercompensation $k = 0.6$, and (c) compensation with $k = 0.8$.

Here, k' is the accelerating convergence coefficient $0 < k' \leq 1$.

From (13)–(14) it should be noticed that the magnitude of the 6n-th harmonics was related to the phase angle between the voltage and the current. When the power factor is near 1, the 6n-th harmonics in i_q is several times larger in magnitude than that in i_d, while the 6n-th harmonics in i_d dominates when the power factor is near 0. According to the different load, $|i_q - i_{q\mathrm{av}}|$ or $|i_d - i_{d\mathrm{av}}|$ will be used. A steady load for identifying the compensation factor is preferred. To determine the zero crossing of the load current, many solutions have been proposed and implemented in the past [2], [7], [12]. Here, in order to get a clear zero crossing of load current, the initial k is set to 1.2 to generate overcompensation and partially reduce the current clamping, and the filtered i_d and i_q are used to reconstruct the load current. For a dynamic load, the notch-type filter tuned at the six times the fundamental frequency can be used to partially eliminate the sixth harmonic component of i_d and i_q. Because the experimental load is a R–L load, a simple first-order low-pass filter (LPF) with the cutoff frequency of twice the output frequency is used, and the coefficients of the filter are adjusted according to the output frequency. Using the LPF-filtered i_d and i_q components, the load current is reconstructed, and is used to

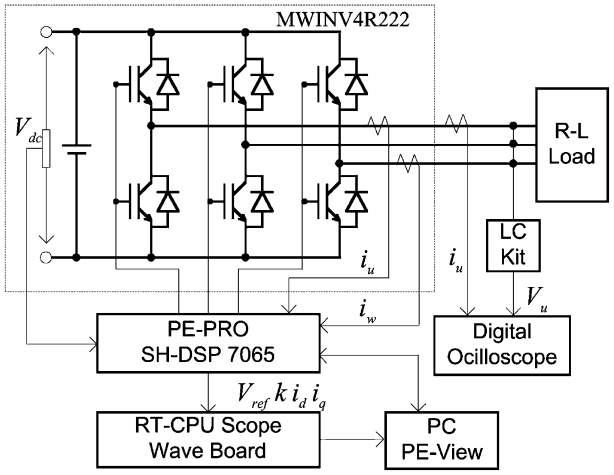

Fig. 7. Test system for identifying the compensation factor.

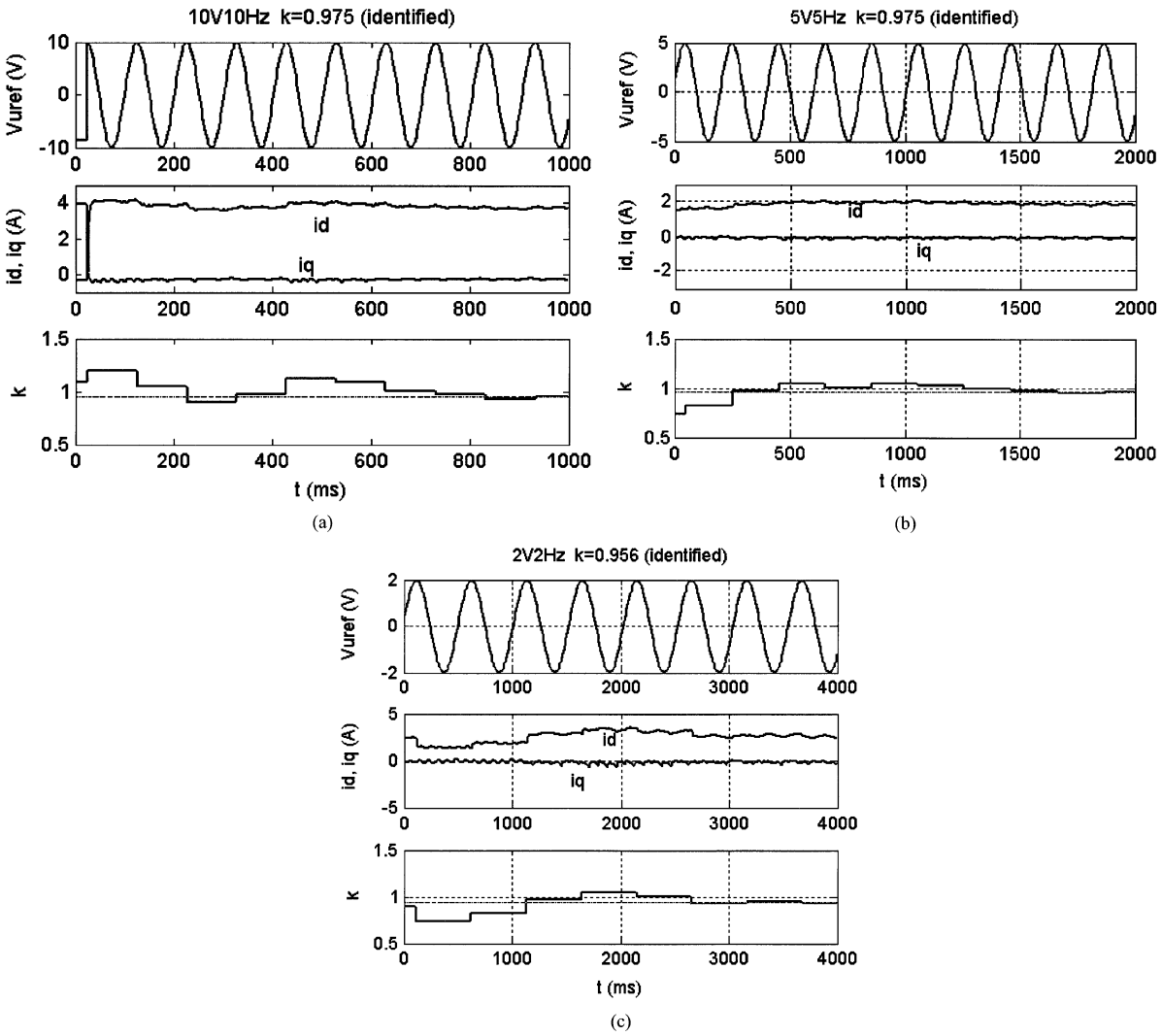

Fig. 8. Identification of compensation factor k: (a) identification under 10 V_{peak} 10 Hz, (b) identification under 5 V_{peak} 5 Hz, and (c) identification under 2 V_{peak} 2 Hz.

determine the current polarity, where the time delay and phase shift of the reconstructed current can be ignored. It should be noted that current clamping becomes a problem if the reference frequency is near zero and at the same time the load current is small, detecting the zero crossing of the current becomes difficult and the compensation will fail.

IV. Results of Simulations and Experiments

Simulation is done at 5 V_{peak} 5 Hz, the load $L = 3$ mH, $R = 2\ \Omega$, carrier frequency is 7 kHz, and the dead time is 4 μs. Fig. 5 shows the reference voltage V_{uref}, output voltage V_u, load current i_u, with its d and q components i_d and i_q. The factor k congregates to 0.8 after 15 periods. Fig. 6 gives the simulation results of overcompensation ($k = 1.0 > 0.8$), undercompensation ($k = 0.6 < 0.8$) and compensation using the identified factor $k = 0.8$. From the simulation results, we can see that both overcompensation and undercompensation will distort the output current and introduce strong 6n-th harmonics in the i_q component. Undercompensation, in particular, causes serious current clamping.

The identification of compensation factor is implemented in a 32-bit RISC DSP (PE-PRO) with a three-phase symmetric R–L load. Current and voltage readings are measured and logged by an integrated development environment (PE-View) and an oscilloscope. This configuration is shown in Fig. 7. The carrier frequency is 7 kHz and the dead time is 4 μs. The load is given by $L = 3$ mH, $R = 3\ \Omega/0.5\ \Omega$. The experiment is done at 10 V_{peak} 10 Hz, 5 V_{peak} 5 Hz and 2 V_{peak} 2 Hz, with the compensation factor congregating to 0.975, 0.975, and 0.956, respectively. The reference voltage V_{uref}, current components i_d and i_q, and compensation factor k from the PE-View are shown in Fig. 8. Actual output waveforms of the experimental voltage and current at 10 V_{peak} 10 Hz, 5 V_{peak} 5 Hz and 2 V_{peak} 2 Hz using the identified compensation factor are shown in Fig. 9.

It should be noted that the resistance voltage drop across the power switches is negligible here since the load current is small. There remains some error between the reference voltage and the actual voltage when the reference voltage is 2 V_{peak} 2 Hz, but the deformation of the output voltage and current is reduced greatly. When the load current is large, the resistance voltage drop across the power switches cannot be ignored. For motor

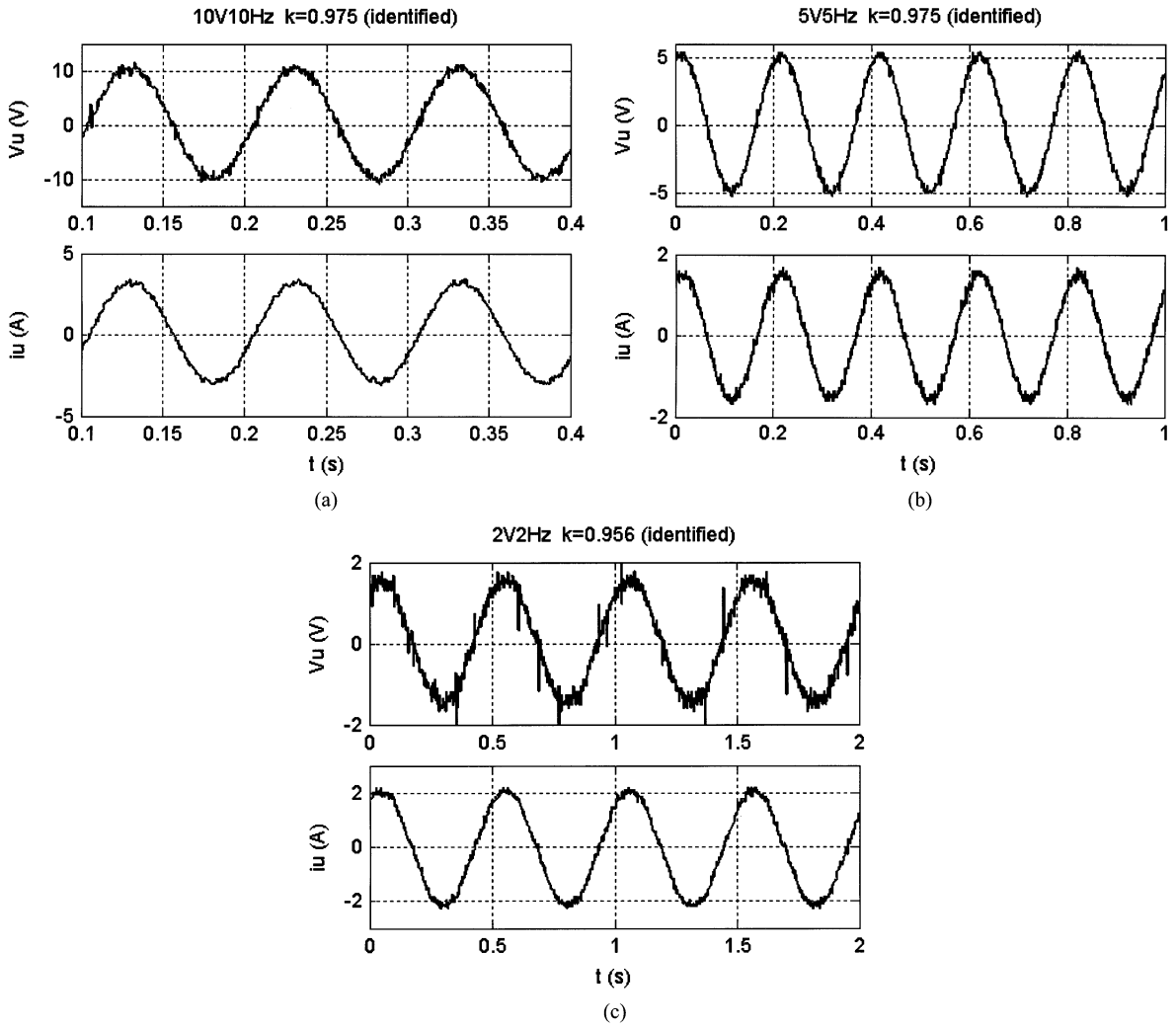

Fig. 9. Compensation results with identified compensation factor: (a) output with $k = 0.975$ under 10 V_{peak} 10 Hz, (b) output with $k = 0.975$ under 5 V_{peak} 5 Hz, and (c) output with $k = 0.956$ under 2 V_{peak} 2 Hz.

control, this conduct resistance can be treated as part of the stator resistance. The identified factors at different frequencies can be compiled in a lookup table, which can be employed to compensate the output voltage for open-loop constant V/f drives.

V. Conclusion

In this study, the 6n-th harmonic current in the synchronous rotating reference frame is minimized to derive the exact compensation factor based on an open-loop system and a L–R load. The compensation factor k is adjusted according to the accumulated error within a half period of the output current. Transient behavior in k during the identification process may cause instability if online identification is used in a closed-loop system. Thus it is preferred to preidentify the compensation factor at different frequencies and by using the identified compensation factor to compose a lookup table. An online smooth adjustment of the compensation factor according to the extracted sixth component is more attractive, and identifying the current polarity according to the reference current is under consideration.

The experiment was mainly done on the low frequency region. The fundamental frequency is less than 15 Hz. It should be feasible at a higher output frequency, but the time delay and phase shift caused by the filter cannot be neglected. The proposed method can accurately identify the compensation voltage introduced by the dead time, turn-on/off delay and the constant voltage drop across the power switches. The main factors attributed to the nonlinearity of VSI inverters and the harmonics of the load currents are analyzed. By minimizing the 6n-th harmonics introduced by the nonlinearity, an accurate compensation voltage can be obtained at low frequencies and low output voltages. Compensation factors can be compiled into a lookup table that can be used for the online open-loop V/f drives. Simulations and experiments illustrated the validity of the proposed method.

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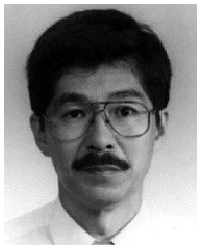
Hengbing Zhao received the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1999.

He joined the Kawamura Laboratory, Department of Electrical and Computer Engineering, Yokohama National University, Yokohama, Japan, in 2000. From 2001 to 2003, he was an Electrical Engineer, and later a Project Leader with Myway Labs Company, Japan. He is presently a Research Associate at the National Research Council, Institute for Fuel cell Innovation, Vancouver, BC, Canada. His research interests include power electronics, design and control of distributed energy systems, and micro fuel cell systems.

Q. M. Jonathan Wu (M'92) received the Ph.D. degree in electrical engineering from the University of Wales, Swansea, U.K., in 1990.

He is a Senior Research Officer and Group Leader of the Microtechnology and Sensing Group, the National Research Council, Institute for Fuel Cell Innovation, Vancouver, BC, Canada. He is also an Adjunct Professor in the School of Engineering Science, Simon Fraser University, Burnaby, BC. From 1992 to 1994, he was with the University of British Columbia, Vancouver, as a Senior Research Scientist. His current research interests include micro fuel cells, alternative micro fabrication technology for MEMS, microsensor development, and microstructure image analysis for MEA characterization.



Atsuo Kawamura (S'77–M'81–SM'96–F'02) was born in Yamaguchi, Japan, in December 1953. He received the B.S.E.E., M.S.E.E., and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1976, 1978, and 1981, respectively.

In 1981, he joined the Department of Electrical and Computer Engineering, University of Missouri-Columbia, Columbia, as a Postdoctoral Fellow, and was an Assistant Professor there from 1983 through 1986. He joined the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama, Japan, in 1986 as an Associate Professor, and in 1996 he became a Professor. His interests are in power electronics, digital control, electric vehicles, robotics, train traction control, etc.

Dr. Kawamura received the IEEE IAS TRANSACTIONS Prize Paper Award in 1988, the Prize Paper Award of the Institute of Electrical Engineers of Japan in 1996, and the IEEE IES TRANSACTIONS Best Paper Awards in 2001 and 2002. He is a member of the IEE of Japan and the Robotics Society of Japan. He was the Conference Chairperson of the IEEE/IAS and IEEJ/IAS joint Power Conversion Conference (PCC-Yokohama) in 1993.