Available online at www.sciencedirect.com
SCIENCE DIRECT®
Journal of Crystal Growth 267 (2004) 592–597
JOURNAL OF CRYSTAL GROWTH
www.elsevier.com/locate/jcrysgro

High-performance InP/GaAsSb/InP DHBTs grown by MOCVD on 100 mm InP substrates using PH_3 and AsH_3

H.G. Liu[a], J.Q. Wu[a], N. Tao[a], A.V. Firth[b], E.M. Griswold[b], T.W. MacElwee[b], C.R. Bolognesi[a,*]

[a] *School of Engineering Science, Simon Fraser University CSDL, 8888 University Drive, Burnaby BC, Canada, V5A 1S6*
[b] *Nortel Networks, 3500 Carling Avenue, Nepean, Ont., Canada, K2H 8E9*

Received 19 February 2004; accepted 16 April 2004

Communicated by T.E. Kuech

Abstract

High-performance MOCVD-grown N-p-N InP/GaAsSb/InP DHBTs based on epitaxial layers deposited on 100 mm InP substrates are reported. The transistors feature the first nearly ideal emitter/base junction characteristics reported for material grown using AsH_3 and PH_3 hydride precursors, a DC current gain $\beta = 30-40$, and a peak cutoff frequency $f_T = 245$ GHz for a $0.5 \times 12\,\mu m^2$ emitter fabricated on a 250 Å lattice-matched carbon-doped base. We discuss layer composition and thickness uniformity, C-doping efficiency as determined by the comparison of SIMS and Hall effect data on bulk $GaAs_{0.5}Sb_{0.5}$ layers, as well as provide SIMS and TEM data for the transistor layers (including a lattice image of the interface between GaAsSb and InP). To our knowledge, the present article provides the first detailed characterization of high-speed InP/GaAsSb/InP DHBTs fabricated on industrially grown epitaxial layers.

Keywords: B2. Semiconducting III–V materials; B3. Electron device manufacture; B3. Heterostructure bipolar transistors

1. Introduction

InP/GaAsSb/InP N-p-N double heterojunction bipolar transistors (DHBTs) have demonstrated wide bandwidths (f_T and f_{MAX} simultaneously exceeding 300 GHz for a 200 Å base layer) with a record $f_T \times BV_{CEO}$ product of >1800 GHz V [1]. These performances are enabled by the simple layer structure allowed by the absence of collector current blocking with the staggered (“type-II”) band lineup [2] at the base-collector heterojunction: with a staggered p-N base-collector heterojunction band alignment, electrons are launched into the widegap InP collector from the p+ GaAsSb base layer, without the complications associated with various grading schemes required to overcome the blocking band discontinuity when otherwise more mature $Ga_{0.47}In_{0.53}As$ base layers are used in DHBTs. The performance and

*Corresponding author. Tel.: 6042915964; fax: 6042914951.
E-mail address: colombo@sfu.ca (C.R. Bolognesi).

0022-0248/$ - see front matter © 2004 Elsevier B.V. All rights reserved.
doi:10.1016/j.jcrysgro.2004.04.035

manufacturability advantages of InP/GaAsSb/InP DHBTs [3] have motivated a number of corporate laboratories to initiate InP/GaAsSb/InP DHBT development programs [4, 5]. Although promising results have recently been reported by workers from *Agilent* with $f_T = 210$ GHz and impressive digital circuit gate delays of 2.7 ps with an AlInAs emitter technology [5], the best published InP/GaAsSb/InP DHBT device results to date still originate from material grown in SFUs MOCVD growth facility using a small Thomas Swan research reactor fitted with lower toxicity TBAs and TBP group V precursors [6,7]. In this context, it is of interest to determine whether research laboratory performances can be replicated on industrially grown epitaxial layers produced in production capable reactors. We report $0.5 \times 12\,\mu m^2$ DHBTs with a peak $f_T = 245$ GHz achieved with a 250 Å base thickness for MOCVD layers grown on 100 mm InP substrates using AsH_3 and PH_3 precursors: this is the highest cut-off frequency ever reported for industrially grown InP/GaAsSb/InP DHBT layers. The present report confirms the feasibility of high-performance InP/GaAsSb/InP DHBTs grown in production capable MOCVD reactors. The work demonstrates that high-quality InP/GaAsSb/InP DHBTs can be implemented whether hydride or alkyl-based group-V precursors are chosen—in fact, the use of AsH_3 for the growth of the base C-doped base layer appears to lead to higher higher hole mobilities. Additionally, the present report shows for the first time that the hydride precursors can be used to grow high-quality InP/GaAsSb emitter-base junctions without having to resort to $Al_{0.48}In_{0.52}As$ emitters as in Ref. [5].

2. Epitaxy and device fabrication

The epitaxial layers used for the present study were grown by MOCVD on 100 mm diameter (1 0 0) semi-insulating InP:Fe substrates at *Nortel Networks* (Ottawa, ON), and processed at the Simon Fraser University Compound Semiconductor Device Laboratory (CSDL). Growth was performed in a horizontal low pressure (76 Torr) reactor using palladium diffused hydrogen as the carrier gas with a total flow rate of 20 l/min. In contrast to the layers grown at SFU (which are produced using TBAs and TBP sources), growth was carried out with AsH_3 and PH_3 precursors, along with a TMSb source. Silicon (Si_2H_6) was used as the donor impurity whereas sulphur (H_2S) is used in the layers grown at SFU. The transistor layers consisted of an n^+ 1000 Å $Ga_{0.47}In_{0.53}As$ cap, a 500 Å InP emitter Si-doped to $1 \times 10^{19}\,cm^{-3}$, a 700 Å InP emitter Si-doped to $3 \times 10^{17}\,cm^{-3}$, a 250 Å $GaAs_{0.51}Sb_{0.49}$ base doped with carbon with CBr_4 to a nominal level of $5 \times 10^{19}\,cm^{-3}$ (resulting in a measured TLM sheet resistance of 1800 Ω/sq), a 2000 Å InP collector doped to $2 \times 10^{16}\,cm^{-3}$ with Si, and a heavily doped 500 Å GaInAs etch-stop layer, and a 3000 Å InP sub-collector doped with Si at $1 \times 10^{19}\,cm^{-3}$. The V/III ratio was maintained to approximately 2 for the growth of $GaAs_xSb_{1-x}$ layers in order to control the alloy mole fraction x, and to 50 for InP. Growth rates of ~2 μm/h were used throughout the structure.

Fig. 1 shows a low-magnification transmission electron micrograph (TEM) of a typical DHBT layer stack revealing smooth layers and interfaces with good thickness control. Fig. 2(a) shows a

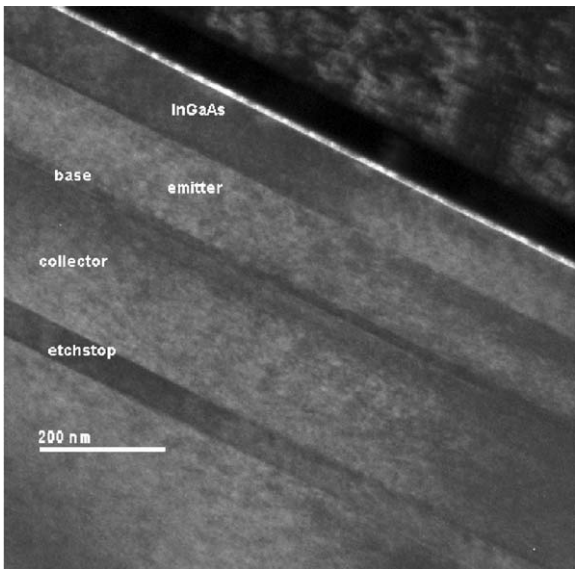

Fig. 1. Low magnification TEM image of typical DHBT layer stack.

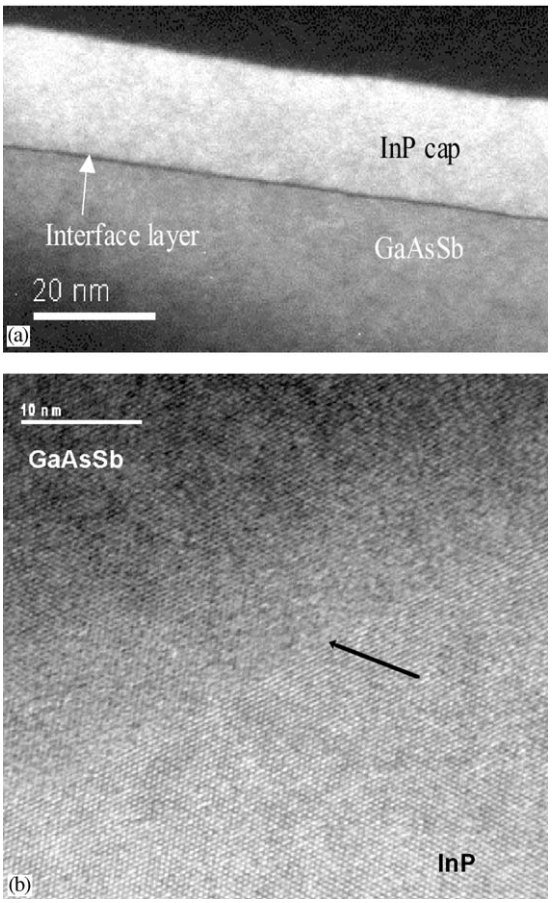

Fig. 2. (a) TEM characterization of the interface between InP and GaAsSb showing a thin ~10 Å interface layer due to strain contrast. (b) 500 K× lattice image of the GaAsSb-on-InP interface region. The arrow marks the interface.

higher magnification image of the interface between GaAsSb and InP: an interface layer of ~10 Å is visible (and independent of the sample tilt in the TEM) most likely due to strain contrast because none of the possible interface III–V bonds are lattice-matched to InP (the possible bonds are In–As, In–Sb, and Ga–P). We note that a similar interface layer is also visible at the InP-on-GaAsSb interface, and that it seems not to depend on the specific gas switching sequence used at the interface (the effects of gas switching on transistor performance lies beyond the scope of the present article and must be addressed in due course in a separate publication). The interface as seen in Fig. 2(a) does not appear to involve an extended grading region, although TEM image contrast is not the best method to assess grading effects. Our electrical data (Section 3) demonstrates good interface control. Fig. 2(b) provides a lattice image of the GaAsSb-on-InP interface region with a ×500 K magnification: because of the lattice strain around the interface, the TEM imaging beam sampling the interface is slightly out of phase when compared to other regions where the lattice image is sharply focused. As shown below in Section 3, the interface structure is of a high electronic quality: for example, the emitter/base diode characteristics features a non-ideality coefficient $n_{EB} = 1.03$ indicative of a nearly ideal N-p junction diode. Fig. 3 shows SIMS profiles for Si, C, and H through the DHBT layers. The peak carbon concentration in the base is $3.8 \times 10^{19}\,cm^{-3}$, roughly 20% under the nominal value: assuming a carbon doping efficiency of 75% (as characterized below), the measured TLM sheet resistance corresponds to a hole mobility of $\sim 49\,cm^2/V\,s$, a value that is comparable to that observed in $Ga_{0.47}In_{0.53}As$ at the same doping level.

The GaAsSb alloy composition was confirmed to be very nearly lattice-matched to InP by SIMS analysis and X-ray rocking curves collected from C-doped GaAsSb bulk layers deposited on

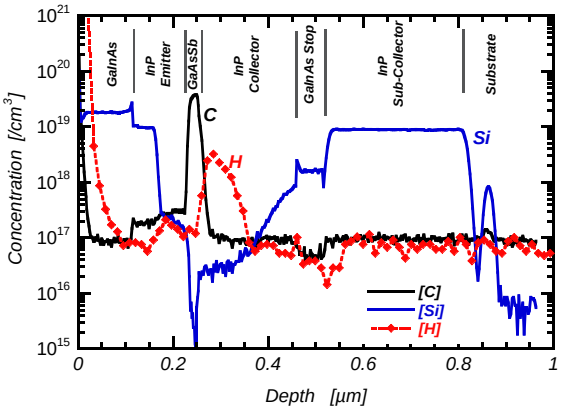

Fig. 3. Silicon, carbon and hydrogen SIMS profiles through the transistor layer stack. A clear silicon outdiffusion is visible from the GaInAs collector etch stop layer. This phenomenon was suppressed in subsequent growths by optimizing the InP collector deposition conditions.

InP: typical XRD results indicate a 161 arcsec separation with respect to the substrate, corresponding to a $x = 0.501$ arsenic solid content. The C-doping efficiency in GaAsSb was characterized on bulk C-doped layers by comparing Hall effect hole concentrations to the SIMS C-concentrations: for a SIMS C-concentration of $4.6 \times 10^{19}\,cm^{-3}$ a free hole concentration of $3.5 \times 10^{19}\,cm^{-3}$ was measured, corresponding to a 75% doping efficiency. SIMS profiling on layers also revealed a low hydrogen concentration of $8 \times 10^{17}\,cm^{-3}$ (or 1.7% of the total C concentration in the layers). In general, characterization of several C-doped GaAsSb layers grown at *Nortel* indicated that hydrogen incorporation remained between 1% and 4% of the total SIMS carbon concentration for carbon levels ranging from 2×10^{19} to $1.4 \times 10^{20}\,cm^{-3}$. The low hydrogen levels may be attributable to the low V/III ratio used during the growth of GaAsSb layers. Note that the quoted hydrogen concentrations are for "as-grown" samples, without any growth interruptions or annealing cycles to drive hydrogen out of the layers. In contrast, GaAs grown under similar conditions shows hydrogen levels that are roughly $10\times$ higher than in GaAsSb (and independent of AsH_3 flow). Wafer rotation was used during growth in order to improve the uniformity of the layers. Lehighton sheet resistance wafer mapping data indicate a $\pm 17\%$ variation between the center and the edge of a 100 mm wafer. For example, a p-type 500 Å GaAsSb layer doped at $5 \times 10^{19}\,cm^{-3}$ with C was characterized by bulk sheet resistance values of $475 \pm 80\,\Omega/sq$, corresponding to a hole mobility of $\sim 52\,cm^2/Vs$, in good agreement with the measured Hall mobility of $47\,cm^2/Vs$. Both values are consistent with the mobility inferred from the TLM sheet resistance value for the actual transistor layers in the previous paragraph. The hole mobility values are higher than the values reported in Ref. [7] for material grown with a TBAs precursor: the improvement may be due to the use of AsH_3 and the concomitant weakening of the CuPt ordering, as discussed in Ref. [8]. Inspection of selective area diffraction patterns indeed revealed the presence of CuPt-type ordering in our material, in a manner and to a degree that are in good agreement with the AsH_3 grown material of Ref. [8]. The GaAsSb thickness and composition variations across a 100 mm diameter wafer were lower than 5% and 1%, respectively.

Contacts to the GaInAs layers were formed by Ti/Pt/Au, and the base contact stack consisted of Pt/Ni/Pt/Au. Air-bridge interconnects were implemented with thick (> 5000 Å) Ti/Au evaporation and lift-off. For this structure, we typically achieved contact resistances of $4\text{-}5 \times 10^{-7}\,\Omega\,cm^2$ for the base contact. The electrode geometry consisted of a 0.7 μm emitter stripe with a 0.1 μm wet etch undercut. The base electrode was self-aligned with 1.2 μm wide contacts on each side of the emitter stripe, and a ~ 0.6 μm undercut. Such critical dimensions are readily achievable in a production environment, and thus provide a realistic assessment of achievable performances for devices produced in an industrial setting.

3. Transistor characterization

The processed transistors typically featured junction non-ideality factors of $n_{EB} = 1.03$ and $n_{BC} = 1.15$ for the emitter/base and base/collector N-p heterojunctions, indicating the formation of very high-quality interfaces between the GaAsSb base and the InP layers. Fig. 4 shows typical transistor Gummel characteristics measured with

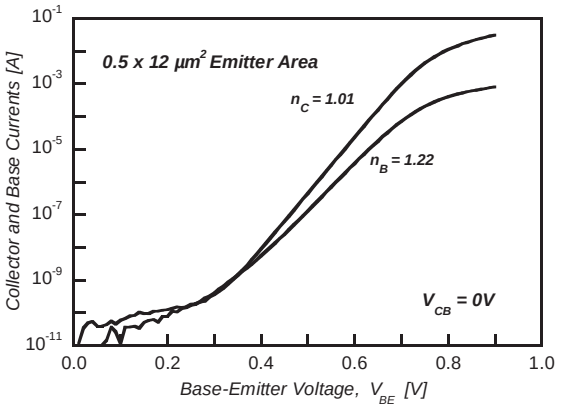

Fig. 4. Room temperature Gummel characteristics featuring a collector and base current current non-ideality factors of $n_C = 1.01$ and $n_B = 1.22$ for a typical unpassivated device with an emitter area of $0.5 \times 12\,\mu m^2$.

$V_{CB} = 0$ V: the collector and base current non-ideality factors are $n_C = 1.01$ and $n_B = 1.22$, indicating that the emitter/base current injection is thermal, and that little recombination takes place at the E/B junction and its periphery despite the lack of an emitter ledge passivation. To our knowledge, such high-quality emitter/base junctions have not been reported before for material grown with AsH_3 and PH_3. Typical current gain values were $\beta \sim 30-40$. Fig. 5 shows representative common-emitter I–V characteristics characterized by a common-emitter breakdown voltage $BV_{CEO} > 6\,V$, a small collector/emitter offset voltage $\Delta V_{CE} = 100$ mV, and a knee-voltage of 0.41 V defined at a collector current density of 1 mA/μm^2 (corresponding to $I_C = 6$ mA in Fig. 5).

The transistor on-wafer dynamic performance was characterized between 1–40 GHz using ground-signal-ground GGB Model 40 A coplanar probes and an HP8510 network analyzer. Fig. 6 shows a peak current gain cutoff frequency $f_T = 245$ GHz (with $f_{MAX} = 275$ GHz, determined by −20 dB/dec extrapolation of Mason's unilateral power gain U) was achieved at a bias of $V_{CE} = 1.6$ V for $J_C = 4.0$ mA/μm^2. To date, this is the highest f_T reported on industrially grown InP/GaAsSb/InP DHBT layers. The present devices show a peak f_T that is slightly lower than the 268 GHz reported by our group for similar layer thicknesses [1] because of the clear silicon tail

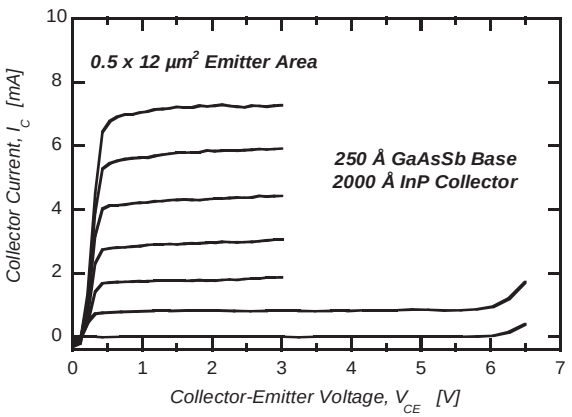

Fig. 5. Representative common-emitter I–V characteristics for a $0.5 \times 12\,\mu m^2$ emitter device with a 250 Å GaAsSb base and a 2000 Å InP collector.

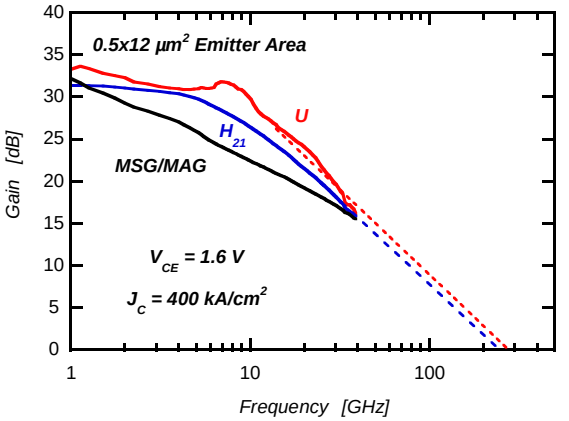

Fig. 6. Microwave performance of a $0.5 \times 12\,\mu m^2$ emitter device biased at $V_{CE} = 1.6$ V and $J_C = 400$ kA/cm^2. Extrapolation of the short circuit current gain and of Mason's unilateral power gain with a −20 dB/dec roll-off yields cutoff frequencies $f_T = 245$ GHz and $f_{MAX} = 275$ GHz.

extending well into the InP collector from the GaInAs sub-collector etch stop layer, as shown in Fig. 3. Although the doping tail was suppressed in subsequent growths by optimizing the InP collector deposition conditions, it results in a partially depleted InP collector in the present set of devices, leading to an effective collector thickness of ~1500 Å. It should be noted that we (SFU) reported $f_T = 250$ GHz for TBAs/TBP grown DHBTs with a 250 Å base and a 1500 Å collector in Ref. [1] —joint consideration of the SIMS and RF characterization data confirms that industrially produced InP/GaAsSb/InP DHBTs can match the performance of laboratory devices [1]. Fig. 7 shows the bias dependence of f_T and f_{MAX}, and reveals that excellent dynamic performances are maintained over a broad range of biasing conditions: Fig. 7(b) shows that maximum oscillation frequencies as high as 330 GHz can be achieved despite the conservative base doping level of 3.8×10^{19} cm^{-3} used in the present devices.

4. Conclusions

We reported the characterization of industrially grown InP/GaAsSb/InP DHBTs with a 250 Å base and cutoff frequencies $f_T = 245$ GHz and $f_{MAX} = 275$ GHz in devices which also feature

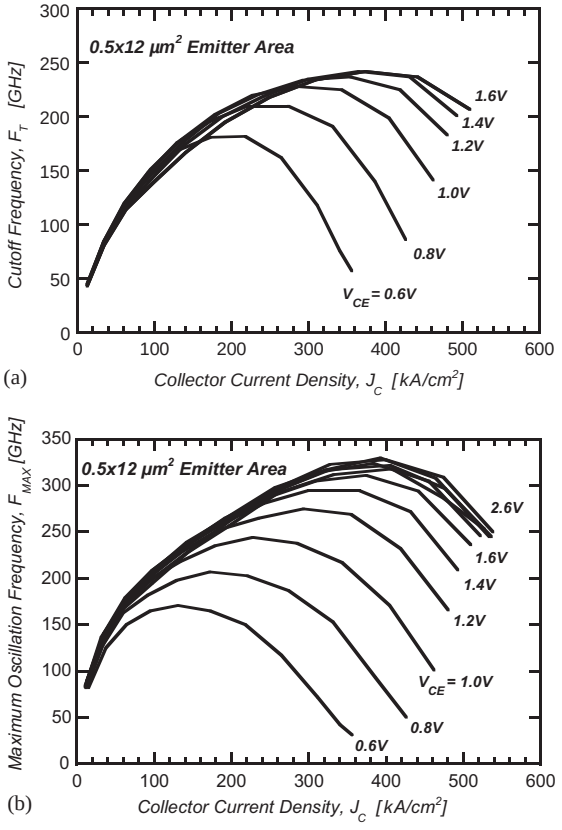

Fig. 7. (a) Bias dependence of the current gain cutoff frequency f_T for V_{CE} values ranging from 0.8 to 1.6V in 0.2V increments; (b)maximum oscillation frequency f_{MAX} for V_{CE} values ranging from 0.8 to 2.6 V in 0.2 V increments. f_{MAX} continues to increase beyond $V_{CE} = 1.6$ V because of the reduction in collector capacitance of the partially depleted collector (see the Si doping profile in Fig. 3).

nearly ideal transistor characteristics in terms of junction and transistor current non-ideality factors. Our demonstration of very high-performance InP/GaAsSb/InP DHBTs on industrially produced epitaxial layers grown on four inch InP substrates marks an important milestone in the maturation of InP/GaAsSb/InP DHBTs, and it confirms the feasibility of a commercial InP/GaAsSb/InP DHBT technology. The present work demonstrates that comparable device performance can be achieved in InP/GaAsSb/InP DHBTs whether TBAs and TBP or AsH_3 and PH_3 sources are utilized: near ideal emitter/base diode characteristics were reported for the first time for material grown with hydride precursors. We have also shown that TEM lattice images from InP–GaAsSb heterojunctions display a relatively featureless interface region that is owed to the variety of possible bonds (In–As, In–Sb, and Ga–P) present at the interface between the two materials.

Acknowledgements

This work was funded by the NSERC Strategic Partnership Program, and by *Nortel Networks*. R. Streater from *Nortel* is gratefully acknowledged for the SIMS data shown in Fig. 3.

References

[1] M.W. Dvorak, C.R. Bolognesi, O.J. Pitts, S.P. Watkins, 300 GHz InP/GaAsSb/InP double HBTs with high current capability and $BV_{CEO} > 6$ V, IEEE Electron. Dev. Lett. 22 (2001) 361–363.

[2] J. Hu, X.G. Xu, J.A.H. Stotz, S.P. Watkins, A.E. Curzon, M.L.W. Thewalt, N. Matine, C.R. Bolognesi, Type II photoluminescence and conduction band offsets of GaAsSb/InGaAs and GaAsSb/InP heterostructures grown by metalorganic vapor phase epitaxy, Appl. Phys. Lett. 73 (1998) 2799–2801.

[3] C.R. Bolognesi, M.W. Dvorak, S.P. Watkins, Type-II base-collector performance advantages and limitations in high-speed NpN double heterojunction bipolar transistors (DHBTs), IEICE Trans. Electron. E86-C (2003) 1929–1934.

[4] R.D. Rajavel, T. Hussain, M.C. Montes, M.W. Sawins, S.T. III, D.H. Chow, Molecular beam epitaxial growth and characterization of InP/GaAsSb/InP double heterojunction bipolar transistors, J. Crystal Growth 251 (2003) 848–851.

[5] S.S. Yi, S.J. Chang, H. Rohdin, M. Hueschen, D. Bour, N. Moll, D.R. Chamberlin, J. Amano, Growth and device performance of InP/GaAsSb HBTs, Extended Abstracts of the 2003 International Conference on Indium Phosphide and Related Materials, 2003, pp. 380–384.

[6] X.G. Xu, J. Hu, S.P. Watkins, N. Matine, M.W. Dvorak, C.R. Bolognesi, Metalorganic vapor phase epitaxy of high-quality $GaAs_{0.5}Sb_{0.5}$ and its application to heterostructure bipolar transistors, Appl. Phys. Lett. 74 (1999) 976–978.

[7] S.P. Watkins, O.J. Pitts, C. Dale, X.G. Xu, M.W. Dvorak, N. Matine, C.R. Bolognesi, Heavily carbon-doped GaAsSb grown for HBT applications, J. Crystal Growth 221 (2000) 59–65.

[8] V. Fink, E. Chevalier, O.J. Pitts, M.W. Dvorak, K.L. Kavanagh, C.R. Bolognesi, S. Hummel, N. Moll, Anisotropic resistivity correlated with atomic ordering in p-type GaAsSb, Appl. Phys. Lett. 79 (2001) 2384–2386.