A Survey on Leakage Control Techniques in Wide-OR Domino Circuits

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***Abstract*— In this paper, we compare different existing keeper techniques for reducing power consumption of wide domino logic circuits. We will compare power consumption plus area overhead of each of these methods, with the conventional keeper circuit. A 16-bit multiplexer circuit, in 0.13µm CMOS technology operating at a frequency of 500 MHz is our test-bench. Simulations show Split-Domino (SD), with 53% less power consumption, and 10.5% more area, has the best performance.**

Index terms—Wide Domino logic, Keeper transistor, Leakage current

I. INTRODUCTION

Wide domino logic [1] refers to domino logic gates with N parallel pull down branches when N>4; that are used to design circuits in microprocessor critical path. Wide fan-in dynamic circuits [2] are used to design high performance register files, ALU front ends, and priority encoders in content addressable memories. At the presence of different noise sources a keeper transistor is used to compensate for any charge losses during evaluation phase. Once very small, keeper transistors in dynamic logic circuits are becoming larger and larger and the contention current is deteriorating the performance and speed of domino logic gates in higher technology nodes. This problem is more severe in wide Domino logic circuits due to the high number of parallel pull-down branches [3].

Fig. 1 shows a 16-bit wide multiplexer with a conventional keeper. Large number of branches in high fan-in domino gates contributes to larger leakage current and discharge of the dynamic node. In sub-deep micron (SDM) technologies the scaling of threshold voltage leads to higher leakage current. This along with denser integration (causing more coupling noise between adjacent wires) both reduce the noise margin of dynamic circuits [4].

In dynamic circuits to measure the reliability of the circuit a figure of merit, called Unity-Gain Noise Margin (UGNM), is defined [5]. UGNM by the definition is the noise level applied to the input of the dynamic gate that results in the same voltage level at the output of the static gate; static inverter in our case here. There are two different methods to measure UGNM:

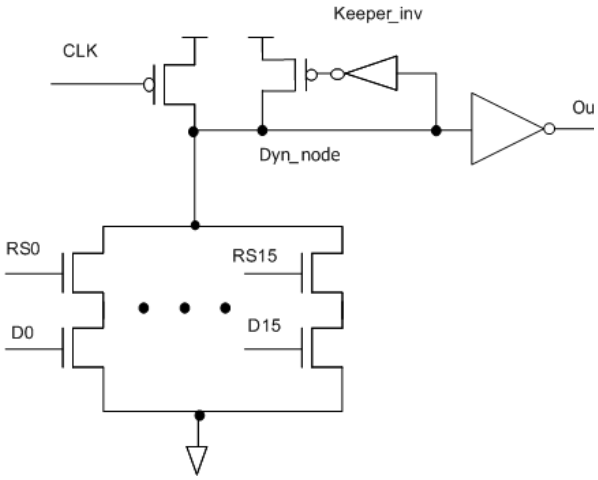

Figure 1 Multiplexer circuit with a conventional keeper

1) Applying a slow ramp at the input and doing transient simulation. The voltage that the output and the applied ramp intersect is UGNM. [6]

2) A square wave input is applied to the input and the output is measured. We used this method for some of the circuit techniques that the first method was not reliable or had to be verified. [5]

In section II, we explain different existing leakage control techniques in wide dynamic multiplexers. In section III, we compare the simulation results of different methods explained in section II. This comparison includes delay, power, energy consumption, and the area for each method.

II. PREVIOUS LEAKAGE CONTROL TECHNIQUES

A. Convetional keeper

Fig. 1 shows the conventional keeper in our 16-bit multiplexer test-bench [7]. The voltage at the dynamic node is susceptible to noise by high-impedance state of the

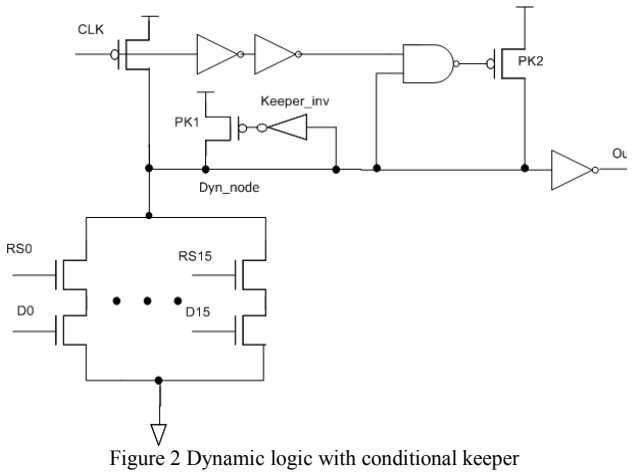

Figure 2 Dynamic logic with conditional keeper

dynamic node during the evaluation mode, when the pull-down path is turned off. This effect can be compensated by reducing the impedance of dynamic node during evaluation, by using a keeper transistor. If the dynamic node voltage is to remain charged, the output of the keeper_inv inverter (Fig. 1) will remain at logic level low. This in turn switches the keeper PMOS transistor on and as a result the dynamic node will be connected to the power supply, providing a mean of voltage drop compensation. The keeper transistor should be large enough to compensate for charge losses and at the same time it should be small enough so that it will not content with NMOS pull-down transistors in the case the pull down network evaluates the dynamic node to logic level zero. Otherwise, the pull down network and keeper transistor compete to drive the dynamic node to two opposite directions, this effect is called contention.

In higher technology nodes smaller threshold voltages that cause exponentially increasing leakage current [7] along with higher levels of noise, due to more aggressive integration, reduce the reliability of the circuit and therefore force designers into using larger keeper transistors to keep up with the target minimum noise margin. Larger keeper transistors in turn increase the contention between pull down network and the keeper transistor. This causes having larger propagation delays and more energy consumption due to higher energy dissipation by keeper transistor and irregularity in dynamic node charging. In the following subsections a few methods from the literature are introduced that can help in reducing the size of or minimizing the impact of already large keeper transistor on the performance of the circuit.

B. Conditional keeper

A conditional keeper (CKP) with variable strength can be used to reduce the contention between keeper transistor and pull-down network [5]. Fig. 2 shows the CKP technique circuit. In this method only a smaller portion of keeper transistors becomes operational during the evaluation phase and the remaining strength of the keeper for target noise margin is entered the circuit only if the dynamic node is to remain at logic level high while floated. Therefore, during the critical phase of evaluation if the output evaluates due to

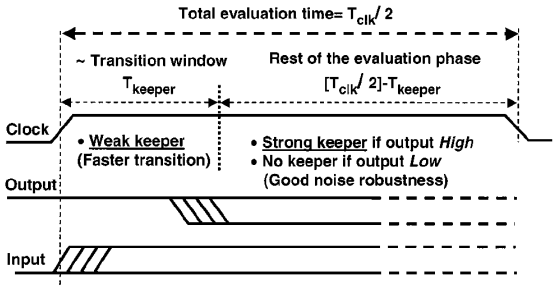

Figure 3 Conditional keeper timing diagram

specific combination of input signals the contention is kept within reasonable limits resulting in faster transitions. At the same time the small keeper transistor, during this time interval, needs to maintain the noise robustness. These requirements must be kept in mind for sizing PK_1 and PK_2 and a trade-off between robustness and speed exists. Fig. 3 shows the timing diagram of the dynamic gate with CKP [5]. Keeper time (T_{keeper}) is known and must be slightly longer that the worst-case output transition time.

To determine the size of two keeper transistors the following guidelines must be followed. The total sum of the width of two keeper transistors equals the width of keeper transistor in conventional technique:

$$W(PK_1) + W(PK_2) = W(PK_0)$$

As mentioned before, for high performance PK_1 must be small but it needs to maintain noise robustness during T_{keeper}, before the second keeper is conditionally fired. First, we determine the UGNM for conventional circuit with the standard keeper. Next for the desired T_{keeper} we size PK_1 to get the same output until the output noise level does not exceed the UGDN level of the conventional case.

C. Split-Domino technique[8]

As already mentioned, there are many parallel branches in a large fan-in dynamic multiplexer gate. These NMOS pull-down branches cause a large amount of leakage current when the dynamic node voltage remains at V_{DD}, not to mention a huge capacitive parasitic that increases the propagation delay as these parasitic must be discharged during an evaluation to zero. Split-domino is a very smart technique that by splitting the pull-down network into smaller groups improves the operation of the gate in both situations [8]. Therefore, in theory we need keeper transistor with a width almost half as much as the conventional circuit. Fig. 4 shows the 16-bit domino multiplexer gate split in two. The circuit overhead is not as much as it might look, as there are two static inverters in the conventional keeper in place of two and three input NAND gates and besides they can be implemented using minimum size transistors. The circuit overhead is almost the same as the conditional keeper technique, if not less.

D. Variable-threshold keeper [9]

Fig. 5 shows the circuit for variable-threshold keeper technique. In this method the body bias voltage of the keeper

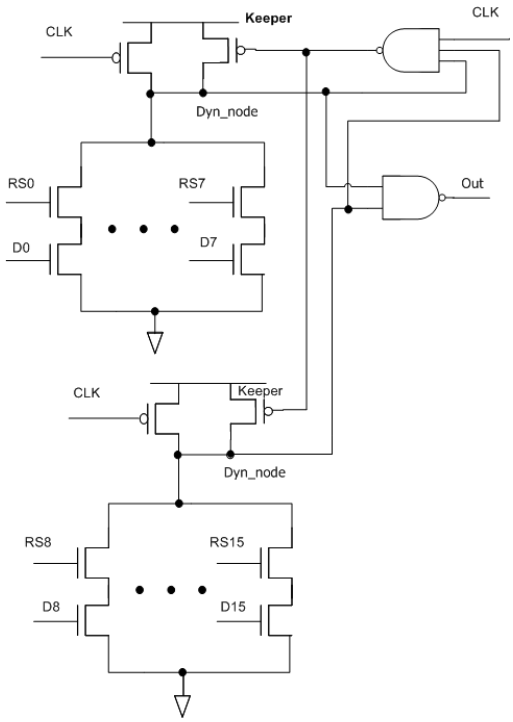

Figure 4 Split Domino technique with pull-down network split in two

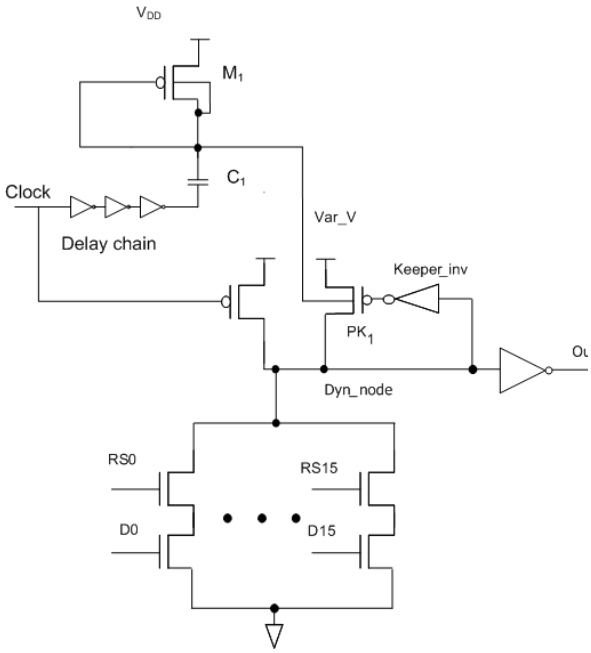

Figure 5 Variable-threshold keeper technique

transistor is controlled by the clock signal. As can be seen in Fig. 5, a delayed clock signal is connected to a diode-connected PMOS transistor through a capacitor, which is connected to the body junction of the keeper transistor operating as a voltage-doubling [9]. The delay of the inverting delay line is determined by the same method as the conditional keeper method. The value of the capacitor C_1 is almost the same as the diffusion capacitance between bulk and drain of PK_1 transistor, and its final value is optimized by simulation. This method is very similar to the CKP technique in principles but the circuit is much simpler, so is the timing diagram to Fig. 3. As we will see in the comparative simulation results, this simplicity also causes this technique to be less efficient compared to CKP. In variable threshold technique the strength of the keeper transistor is controlled only by the clock signal and not dynamic node voltage and as a result always after T_{keeper} window the strong keeper engages in the variable threshold keeper. Fig. 6 shows the simulation results for the dynamic multiplexer test bench. The energy per cycle (PDP) of the circuit is more efficient for larger keeper sizes and for a keeper size of 9µm the variable threshold keeper circuit consumes 12.5% less energy than that of conventional keeper. This can be advantageous when higher noise margins are required and this method could help reduce the power and energy consumption of the system.

III. Performance Comparison of Presented Methods

Simulations are performed in 0.13 µm technology at 500 MHz frequency. The fall/rise times of the waveforms were set to 50pS. Considering the application of wide multiplexer gates the load capacitance of the output static inverter of the dynamic gate was set to the gate capacitance of a NMOS transistor with a width of 20µm, which is an estimate for an ALU bus [6]. To ensure correct operation of the multiplexer circuit during evaluation phase, when the clock is high, two worst-case conditions must be fulfilled [5]:

1) Worst-case delay (hig-to-low transition):
RS0 = 1, D0 = 1, RS1 ... RS15 = 0, and D1 …D15 = 0.

2) Wrost-case noise (where dynamic output should remain high): RS0…RS15 = 0 + worst-case dc noise and D0…D15 = 1

TABLE I. SIMULATION RESULTS FOR DIFFERENT KEEPER TECHNIQUE

	Delay	Power	Energy	Area over-head
Conventional	1	1	1	1
Conditional keeper	0.85	0.82	0.70	1.047
Split-Domino (SD)	0.73	0.65	0.47	1.105
Variable threshold (VT)	0.95	0.91	0.87	1.1

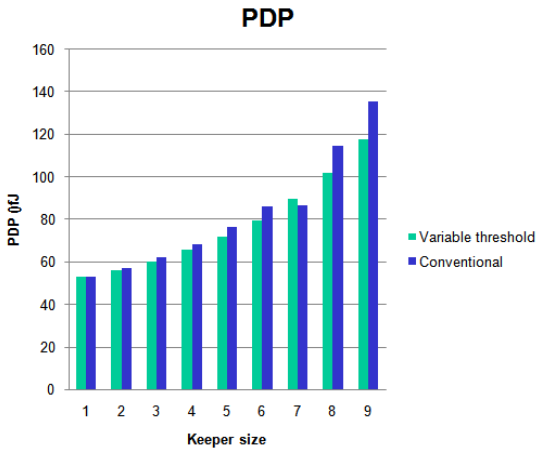

Figure 6 simulation results for variable threshold keeper technique for different keeper sizes

Simulations were performed at the worst-case process leakage corner FNSP (Fast NMOS, Slow PMOS) [7]. To compare different presented techniques a minimum requirement UGNM of 200mV was set as the target. Table I shows the simulation results. The values in the table are normalized to the parameters of the conventional keeper technique. SD technique gives us an energy saving of 53%.

IV. CONCLUSION

Split-Domino method has the best performance among others. SD has a power saving of 53%; this involves only 10.5% area overhead. SD method can be used to divide parallel pull-down branches further (more than two sections) to achieve more power saving.

Variable-threshold keeper can be advantageous when higher noise margins are required. This is due to the fact that it has a better performance for larger keeper sizes (Fig. 6); which is the case for achieving higher UGNM. Therefore, this method could help reduce the power and energy consumption for the required noise performance.

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