Low Power High Performance Keeper Technique for High Fan-in Dynamic Gates

Farhad Haj Ali Asgari, and Majid Ahmadi, Jonathan Wu
Electrical and Computer Engineering Department
University of Windsor
Windsor, Ontario, Canada
{hajali, ahmadi,jwu}@uwindsor.ca

***Abstract*— This paper presents a new technique which combines Variable-Threshold (VT) keeper with Split-Domino (SD) logic technique to improve the power performance. The proposed technique yields 9-14% energy reduction, with 10% area overhead. We will compare the proposed method with the-state-of-the art for reducing leakage current in domino logic circuits. A 16-bit multiplexer circuit, in 0.13µm CMOS technology operating at 500 MHz is used as our test-bench.**

Index terms—Wide/High Fan-in Domino logic, Keeper, Leakage current

I. INTRODUCTION

Wide domino logic [1] refers to domino logic gates with a minimum fan-in of four. They are used in microprocessor critical path circuits. Wide fan-in dynamic circuits [2] are used to design high performance register files, ALU front ends, fast carry look-ahead circuits, and priority encoders in content addressable memories. At the presence of different noise sources a keeper transistor is used to compensate for any charge losses during evaluation phase. Once very small, keeper transistors in dynamic logic circuits are becoming larger and the contention current deteriorates the performance of domino logic gates in higher technology nodes. This problem is more critical in wide Domino logic circuits. [3].

Fig. 1 shows a 16-bit wide multiplexer with a conventional keeper. Large numbers of branches in high fan-in domino gates contribute to larger leakage current and discharge of the dynamic node. In sub-deep micron (SDM) technologies the scaling of threshold voltage leads to higher leakage current. This along with denser integration (causing more coupling noise between adjacent wires) both reduce the noise margin of dynamic circuits [4].

In dynamic circuits to measure the reliability of the circuit a figure of merit, called Unity-Gain Noise Margin (UGNM), is defined [5]. UGNM by the definition is the noise level applied to the input of the dynamic gate that results in the same voltage level at the output of the static gate; static inverter in our case here. There are two different methods to measure UGNM:

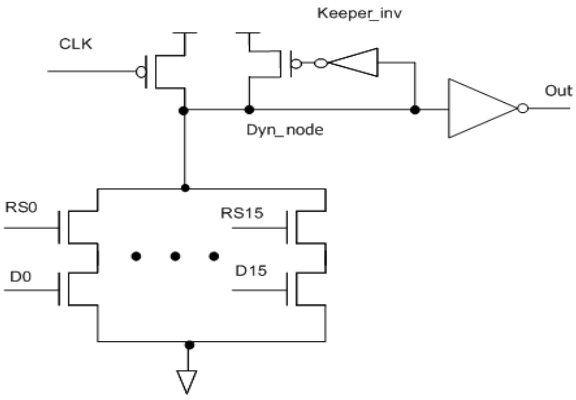

Figure 1 Multiplexer circuit with a conventional keeper

1) Applying a slow ramp at the input and doing transient simulation. The point that the output and the applied ramp intersect is UGNM. [6]

2) Applying a square wave at the input and looking at output. [5] We used this method for some of the circuit techniques that the first method was not reliable or had to be verified.

In the following section, we explain different existing keeper techniques in wide dynamic multiplexers. In section III, we introduce a technique to improve the gate performance of the Split-Domino technique from section II. In section IV, the presented and proposed methods are compared regarding delay, power, energy consumption, and circuit area.

II. PREVIOUS LEAKAGE CONTROL TECHNIQUES

A. Convetional keeper

Fig. 1 shows our 16-bit multiplexer test-bench with the conventional keeper [7]. The voltage at the dynamic node is susceptible to noise by high-impedance state of the dynamic node during the evaluate mode, when the pull-down path is turned off. This effect can be compensated by reducing the

This work was supported in part by the Natural Scientific and Engineering Research Council of Canada

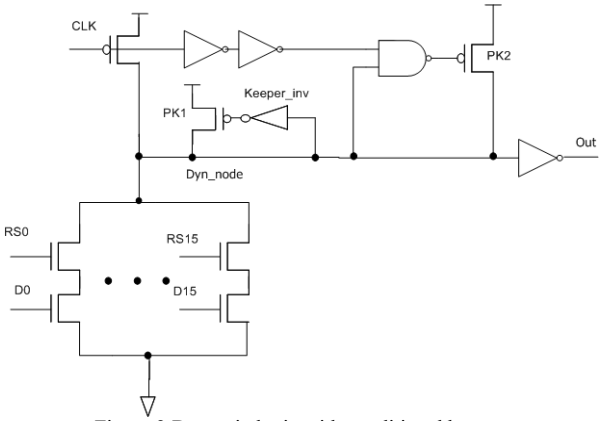

Figure 2 Dynamic logic with conditional keeper

impedance of dynamic node during evaluation. This can be accomplished by a keeper transistor. If the dynamic node voltage is to remain charged, the output of the keeper_inv inverter (Fig. 1) will remain at logic level low. This in turn switches the keeper PMOS transistor on and as a result the dynamic node will be connected to the power supply, compensating any voltage drop. The keeper transistor size should be large enough to compensate for charge losses at dynamic node. At the same time it should be small enough to prevent competition with pull-down network in case the NMOS network is to evaluate to logic level zero. Otherwise, the pull down network and keeper transistor compete to drive the dynamic node to two opposite directions, this effect is called contention.

In higher technology-nodes smaller threshold voltages that cause exponentially increasing leakage current [7] along with higher levels of noise, due to more aggressive integration, reduce the reliability of the circuit and therefore force designers into using larger keeper transistors to keep up with the target minimum noise margin. Larger keeper transistors in turn increase the contention between pull down network and the keeper transistor causing larger propagation delays and more energy consumption due to higher energy dissipation by keeper transistor and irregularity in dynamic node charging. In the following subsections a few methods from the literature are introduced that can help in reducing the size of or minimizing the impact of already large keeper transistor on the performance of the circuit.

B. Conditional keeper[5]

A conditional keeper (CKP) with variable strength can be used to reduce the contentions between keeper transistor and pull-down network [5]. Fig. 2 shows the CKP technique circuit. In this method only a smaller portion of keeper transistors becomes operational during the evaluation phase and the remaining strength of the keeper for target noise margin is entered the circuit only if the dynamic node is to remain at logic level high while floated. Therefore, during the critical phase of evaluation if the output evaluates due to specific combination of input signals the contention is kept within reasonable limits resulting in faster transitions. At the same time the small keeper transistor during this time interval needs to maintain the noise robustness. These requirements

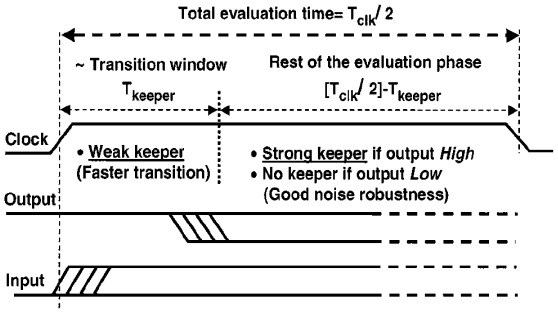

Figure 3 Conditional keeper timing diagram [5]

must be kept in mind for sizing PK_1 and PK_2 and a trade-off between robustness and speed exists. Fig. 3 shows the timing diagram of the dynamic gate with CKP [5]. Keeper time (T_{keeper}) is known and must be slightly longer that the worst-case output transition time.

To determine the size of two keeper transistors the following guidelines must be followed. The total sum of the width of two keeper transistors equals the width of keeper transistor in conventional technique:

$$W(PK_1) + W(PK_2) = W(PK_0)$$

As mentioned before, for high performance PK_1 must be small but it needs to maintain noise robustness during T_{keeper}, before the second keeper is conditionally fired. First, we determine the UGNM for conventional circuit with the standard keeper. Next for the desired T_{keeper} we size PK_1 to get the same output until the output noise level does not exceed the UGDN level of the conventional case.

C. Split-Domino technique[8]

As already mentioned, there are many parallel branches in a large fan-in dynamic multiplexer gate. These NMOS pull-down branches cause a large amount of leakage current when the dynamic node voltage remains at V_{DD}, not to mention a huge capacitive parasitic that increases the propagation delay as these parasitic must be discharged during an evaluation to zero. Split-domino is a very smart technique that by splitting the pull-down network into smaller groups improves the operation of the gate in both situations [8]. Therefore, in theory we need keeper transistor with a width almost half as much as the conventional circuit. Fig. 4 shows the 16-bit domino multiplexer gate split in two. The circuit overhead is not as much as it might look, as there are two static inverters in the conventional keeper in place of two and three input NAND gates and besides they can be implemented using minimum size transistors. The circuit overhead is almost the same as the conditional keeper technique, if not less.

D. Variable-threshold (VT) keeper [9]

Fig. 5 shows the circuit with VT keeper technique. In this method the body bias voltage of the keeper transistor is controlled by the clock signal. A delayed clock signal is connected to a diode-connected PMOS transistor through a capacitor. The PMOS and capacitor (connected to the body of the keeper transistor) operates as a voltage doubling [9]. The

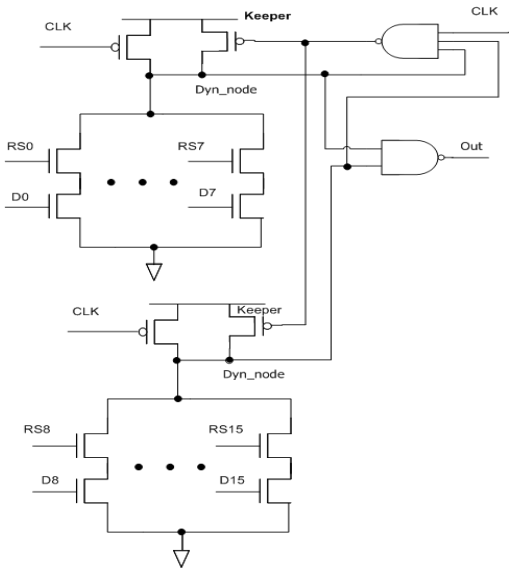

Figure 4 Split Domino technique with pull-down network split in two

delay of the inverting delay line is determined by the same method as the conditional keeper method. The value of the capacitor C_1 is almost the same as the diffusion capacitance between bulk and drain of PK_1 transistor and optimized by simulation. This method is very similar to the CKP technique in principles but the circuit is much simpler. As we will see in the comparative simulation results, this simplicity also causes this technique to be less efficient compared to CKP. In variable threshold technique dynamic node voltage does not control the strength of the keeper. As a result the strong keeper always engages in the variable threshold keeper. Fig. 6 shows the simulation results for the dynamic multiplexer test bench with VT keeper technique. The energy per cycle (PDP) of the circuit is more efficient for larger keeper sizes and for a keeper size of 9µm the variable threshold keeper circuit consumes 12.5% less energy than that of conventional keeper.

III. SPLLIT-DOMINO WITH VARIABLE THRESHOLD KEEPER

From simulations, the required keeper size for the split Domino keeper circuit - to have similar robustness as conventional gate with a UGNM of 200mV - resulted to be 3.6µm. Fig. 6 shows an energy consumption improvement of around 5 to 6% for keeper size in this range. This fact and the simple structure of variable threshold keeper with small circuit overhead makes this method attractive as a technique to be combined with split Domino scheme to gain further power/energy saving. SD technique is more efficient for higher input fan-in [7]. As a result, we can take advantage of another method to further improve the performance of the individual clusters in a SD domino circuit. We suggest a combination of two techniques to further improve the performance of both techniques and SD in particular. Finally, the simulation results for different performance parameters for different keeper techniques are presented in the following subsection.

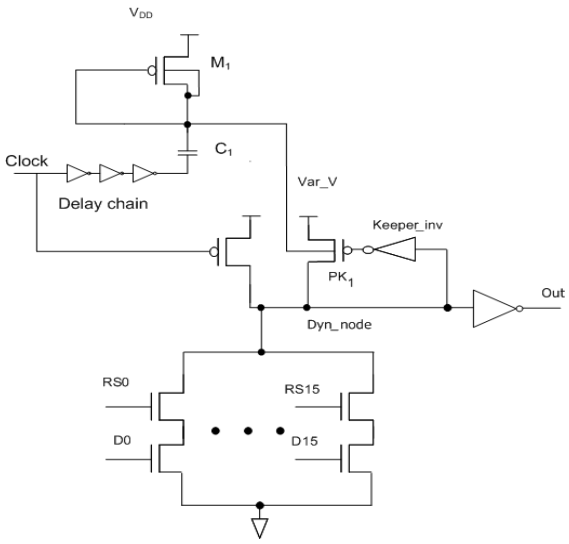

Figure 5 Variable Threshold keeper

A. *Performance Comparison of Presented Methods*

We performed simulation in 0.13 µm technology at 500 MHz The gate capacitance of a NMOS transistor with a width of 20µm, which is an estimate for an ALU bus [6]. To ensure correct operation of the multiplexer circuit during evaluation phase, when the clock is high, two worst- case conditions must be fulfilled [5]:

1) Worst-case delay (hig-to-low transition):

RS0 = 1, D0 = 1, RS1 ... RS15 = 0, and D1 …D15 = 0.

2) Wrost-case noise (where dynamic output should remain high): RS0…RS15 = 0 + worst-case dc noise and D0…D15 = 1

TABLE I. NORMALIZED RESULTS FOR DIFFERENT KEEPER TECHNIQUES

	Delay	Power	Energy	Area over-head
Conventional	1	1	1	1
Conditional keeper	0.85	0.82	0.70	1.047
Split-Domino (SD)	0.73	0.65	0.47	1.105
Variable threshold (VT)	0.95	0.91	0.87	1.1
SD + VT	0.714	0.627	0.448	1.21

Keepers sized at the worst-case process leakage corner FNSP to meet the assigned noise requirements [5]. Dynamic circuits have the smallest noise margin in the FNSP corner where the NMOS transistors have a low threshold and the

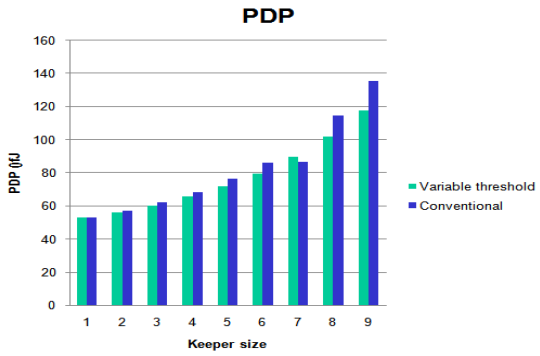

Figure 6 Simulation results for variable threshold keeper technique for different keeper sizes

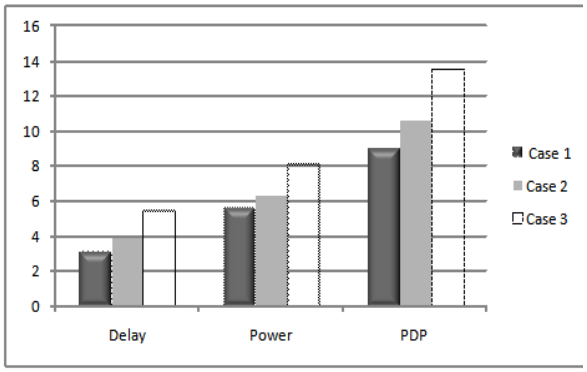

Figure 7 Proposed method performance improvement over conventional SD for three different delay constrains in percent

PMOS keepers are weak. To compare different presented techniques a minimum required UGNM of 200mV was set as the target. Table I shows the simulation results. The values in the table are normalized to the parameters of the conventional keeper technique. SD technique gives us an energy saving of 53%. We have 4.5% further reduction in energy consumption using variable threshold voltage, compared to simple SD (table I).

B. *Performance of Variable Threshold Method for Higher UGNMs*

As can be seen in Fig. 6, the variable threshold keeper technique has a better performance when keeper transistor is larger. It should be noticed that in general, in noisy conditions a noise margin as high as possible is required. A higher UGNM dictates a larger keeper transistor, which is desirable by variable threshold keeper method and translates into higher performance and energy saving. Based on the above discussion the SD and SD/VT dynamic multiplexers were simulated with a target UGNM of 500mV. The simulation results are tabulated in table II. The second row shows performance improvement for higher target UGNM.

Table II. PERFORMANCE IMPROVEMENT OF SD/VT FOR LARGER NOISE MARGINS

UGNM (mV)	Delay (pS)	Power (µW)	Energy (fJ)
200	1.6%	3.1%	4.5%
500	3.1%	6.2%	9%

We designed and simulated the circuit for looser delay constraints. Fig. 7 shows the results for three different propagation delay conditions. The propagation delay of the case 3 is 15% more than in case 1. With aiming at a larger delay at this degree we get 13.5% energy saving compared to conventional SD technique. This indicates in less performance critical systems the proposed technique consumes less power and energy.

IV. CONCLUSION

Split-Domino method has the best performance among others. SD has a power saving of 53%, this involves only 10.5% area overhead. SD method can be used to divide parallel pull-down branches further (more than two sections) to achieve more power saving. SD with variable-threshold keeper can be advantageous when higher noise margins are required. This is due to the fact that it has a better performance for larger keeper sizes (Fig. 6); the case for achieving higher UGNM. It is also more power efficient when delay can be relaxed. Therefore, this method could help reduce the power and energy consumption for the required noise performance when delay-power trade-off is on the table.

REFERENCES

[1] L. T. Clarke, G. F. Taylor, "High fan-in circuit design", IEEE Journal of Solid-State Circuits, vol. 31, Issue 1, January 1996, pp.91-96.

[2] C. Kwong, B. Chatterjee, and M. Sachdev, "Modeling and designing energy-delay optimized wide domino circuits," ISCAS '04. Proceedings of the 2004 International Symposium on Circuits and Systems, 2004. Volume 2, 23-26 May 2004 pp. II - 921-4

[3] V. De and S. Borkar, "Technology and design challenges for low power and high performance," *Proc.of Intl.* Symp. on Low Power Electronics and Design, pp.163-168, SanDiego, CA, Aug. 1999.

[4] David A. Hodge, Horace G. Jackson, and Resve A. Saleh, "Analysis na design of digital integrated circuits: In deep submicron technoloty, third edition", McGraw Hill higher education, p. 69., 2005.

[5] A. Alvandpour, , R.K. Krishnamurthy, K. Soumyanath, and S.Y. Borkar, , "A sub-130-nm conditional keeper technique," IEEE journal of solid-state circuits, Volume 37, Issue 5, May 2002 pp. 633 - 638

[6] S. Naraghi, "Reduced swing Domino techniques for low power and high performance arithmetic circuits", Master of Science thesis, Electronic and Computer Engineering department, University of Waterloo, Waterloo, Ontario, p.53., 2004

[7] C. Hua, W. Hwang, and C. Chen, "Noise–tolerant XOR-based concitional keeper for high fan-in dynamic circuits", ISCAS 2005. IEEE International Symposium on Circuits and Systems, 23-26 May 2005 pp. 444 - 447 Vol. 1

[8] M. Elgebaly, M. Sachdev, "A leakage tolerant energy efficient wide domino circuit technique," Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on, Volume 1, 4-7 Aug. 2002 pp. I - 487-90 vol.1.

[9] A. Amirabadi, A. Afzali-Kusha, Y. Mortazavi, and M. Nourani, "Clock delayed domino logic with effiecient variable threshold voltage keeper," IEEE transactions on VLSI systems, vol. 15, no.2, February 2000.